REMARKS/ARGUMENTS

Applicant thanks the Examiner for total consideration given the present application.

Claims 1-17 are currently pending in the present application. Claims 1-14 are originally presented, and claims 15-17 are newly added.

Rejection under 35 U.S.C. § 102

Claims 1-4 and 9-14 under 35 USC § 102(e) as being anticipated by ***Krauch et al.*** (U.S. Patent No. 6,668,341). Applicant respectfully traverses the rejection.

In regard to independent claims 1 and 9, Examiner alleged that the ***Krauch et al.*** reference discloses a method of recording and reproducing information as claimed by Applicant. Specifically, Examiner considered the cell and cell latches in ***Krauch et al.*** as the block and the pages as claimed in claims 1 and 9 of the present application, respectively. Applicant respectfully submits that the ***Krauch et al.*** reference does not disclose the "pages' claimed in independent claims 1 and 9. One feature of applicant's invention is to realize high-speed error correction of a specific part of information by physically divide a recording area of a recording medium into small pages, and partition the recording area into separate physical blocks, each having a plurality of the pages so that information is recorded and reproduced in units of the blocks to and from the recording medium. Each individual page, according to the present invention, comprises, as shown in Fig. 1, a data area, an added information area, a logical address part, and an error correcting redundant part. The "pages" as referred to by Examiner in ***Krauch et al.*** are the storage elements (Fig. 2, elements 10, 12), which are merely single bit latches as disclosed in column 3, lines 36-42. As can be seen, the "pages" in ***Krauch et al.*** relied on by Examiner are totally different in structure than the pages as claimed in the present invention. In contrast, the "pages" as recited in claims 1 and 9 are physical space capable of storing multi-bit data, information, logical address, and error correcting redundant information as shown in Fig. 1 of the present application. Accordingly, for at least the reasons stated above, independent claims 1 and 9 are not anticipated by ***Krauch et al.*** as alleged, and the rejection under 35 USC § 102(e) should be withdrawn.

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Dependent claims 2-4, and 10-14 are dependent on independent claims 1 and 9, respectively. Claims 2-4, and 10-14 are patentably distinct from the ***Krauch et al.*** reference for at least the reasons as discussed above for independent claims 1 and 9. Accordingly, applicant believes dependent claims 2-4, and 10-14 are not anticipated by ***Krauch et al.*** as alleged, and the rejection under 35 USC § 102(e) should also be withdrawn.

Rejection under 35 U.S.C. § 103

Claims 5-8 stand rejected under 35 USC § 103(a) as being unpatentable over ***Krauch et al.*** (U.S. Patent No. 6,668,341) in view of ***Flaherty et al.*** (U.S. Patent No. 5,128,944). Applicant respectfully traverses this rejection.

The main objective of the ***Krauch et al.*** invention is to obtain error correction in storage cell without such a high overhead in area consumption. If the multi-bit logical addresses of ***Flaherty et al.*** were to be used to replace the single-bit storage elements of ***Krauch et al.***, as suggested by the Examiner, it would totally contradict the main objective of the ***Krauch et al.*** invention. Accordingly, one having ordinary skill in the art would not have been motivated to incorporate the multi-bit logical addresses of ***Flaherty et al.*** for the single-bit storage elements of ***Krauch et al.*** Applicant respectfully submits that dependent claims 5-8 are not obvious over ***Krauch et al.*** in view of ***Flaherty et al.*** as alleged for at least the stated reasons above, and the rejection under 35 USC § 103(a) should be withdrawn.

In view of the above reasons, applicant believes that the rejection of claims 1-4 and 9-14 under 35 USC § 102(e), and the rejection of claims 5-8 under 35 USC § 103(a) have been overcome. Accordingly, claims 1-14, as originally presented, are now in condition for allowance.

New claims

New claim 15 is added to emphasize the feature, *inter alia*, "When reading of the logical addresses in all blocks has completed, the logical/physical address translation table creating

procedure ends." Support of this feature can be found in the present application on page 8, lines 5-6. No new matter has been presented.

New claim 16 is added to further emphasize the feature of, *inter alia*, creating the address translation table has the benefit of speedy parity checking as compared to the conventional Reed-Solomon error checking method. Support of this feature can be found in the present application on page 8, lines 7-14. No new matter has been presented.

New claim 17 is added to emphasize the feature, *inter alia*, the "pages" of the present invention store logical addresses having multi-bit data, rather than a "single-bit" latch as shown in ***Krauch et al***. Support of this feature can be found in the present application on page 7, lines 24-26. No new matter has been presented.

CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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